

P11159-201AS



Small package and high resolution encoder module

The P11159-201AS is an encoder module that incorporates a red LED and a photo IC designed specifically for optical encoders. This encoder module detects the displacement or rotation angle of the object. When the slit optical pattern attached to the object moves between the LED and photo IC, the 4-element photodiode in the photo IC reads the slit optical pattern, and then outputs the pattern signals (phase A and phase B).

Features

- High resolution: 0.05 mm (2-phase output)
- Positioning pin for easy alignment
- Small package
- Suitable for lead-free flow soldering
- Low power consumption

Applications

- Rotary encoder
- Linear encoder

Absolute maximum ratings (Ta=25 °C)

	Parameter	Symbol	Condition	Value	Unit
Input (LED)	Forward current*1	If max		25	mA
	Reverse voltage	Vr max		5	V
	Power dissipation	P		100	mW
Output (photo IC)	Supply voltage	Vcc max		-0.5 to +7	V
	Output voltage	Vo max		-0.5 to Vcc + 0.5	V
	Output current	Io max		4	mA
	Power dissipation*2	P		250	mW
Operating temperature		Topr	No dew condensation*3	-40 to +85	°C
Storage temperature		Tstg	No dew condensation*3	-40 to +90	°C

*1: Forward current decreases at a rate of 0.5 mA/°C above Ta=55 °C

*2: Power dissipation decreases at a rate of 3.1 mW/°C above Ta=25 °C

*3: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Electrical and optical characteristics (Ta=25 °C, Vcc=5 V, unless otherwise noted)

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input (LED)	Forward voltage	V _F	I _F =10 mA	-	1.9	2.4	V
	Reverse current	I _R	V _R =5 V	-	-	10	μA
	Peak emission wavelength	λ _p	I _F =10 mA	-	650	-	nm
Output (photo IC)	Operating supply voltage	V _{CC}		3.0	-	7.0	V
	Low level output voltage	V _{OL}	I _{OL} =1 mA	-	-	0.4	V
	High level output voltage	V _{OH}		4.5	-	-	V
	Supply current	I _{CC}	V _{OA} =V _{OB} =L	-	6.0	10	mA
Transfer characteristics	Duty ratio* ⁴	t _{AH} /t _{AP}	I _F =5 mA, f=10 kHz	35	50	65	%
		t _{BH} /t _{BP}		35	50	65	%
	Phase difference* ⁴	θ _{AB}	I _F =5 mA, f=10 kHz	60	90	120	degree
	Rise time	t _r	I _F =5 mA, C _L =10 pF	-	0.5	2	μs
	Fall time	t _f	I _F =5 mA, C _L =10 pF	-	0.04	0.3	μs
	Maximum response frequency* ⁴ * ⁵	f _{max}	I _F =5 mA	50	-	-	kHz

*4: Measured when recommended slits are used in specified position

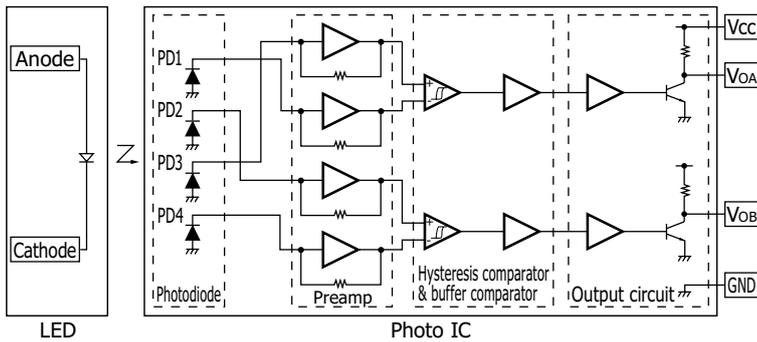
Response frequency f is the reciprocal of the time required to move one pitch.

*5: Maximum frequency at which no error occurs in the output transition sequence (See operation timing diagram.)

Note: Connect a capacitor of 0.1 μF or more between V_{CC} and GND terminal.

Block diagram, truth table

The output of the photo IC for encoder is 2-phase digital output (TTL compatible) consisting of phase A and phase B. Phase A (V_{OA}) shows which of PD1 or PD3 is receiving more light, and phase B (V_{OB}) shows which of PD2 or PD4 is receiving more light.

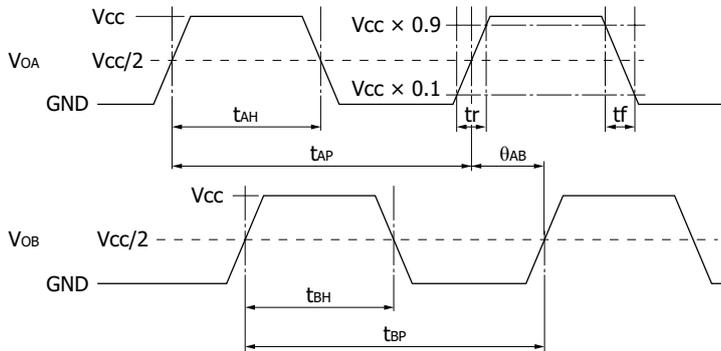


Input		Output	
		V _{OA}	V _{OB}
PD1 < PD3	PD2 > PD4	Low	Low
PD1 < PD3	PD2 < PD4	Low	High
PD1 > PD3	PD2 > PD4	High	Low
PD1 > PD3	PD2 < PD4	High	High

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Operation timing diagram

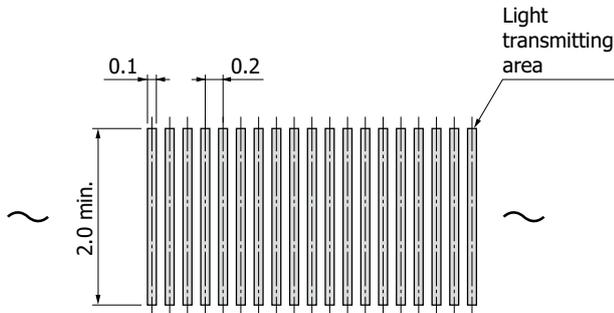
Measured when the slits move at a constant speed towards you from the inner side as viewed from the front, in the middle left drawing in "Dimensional outline".



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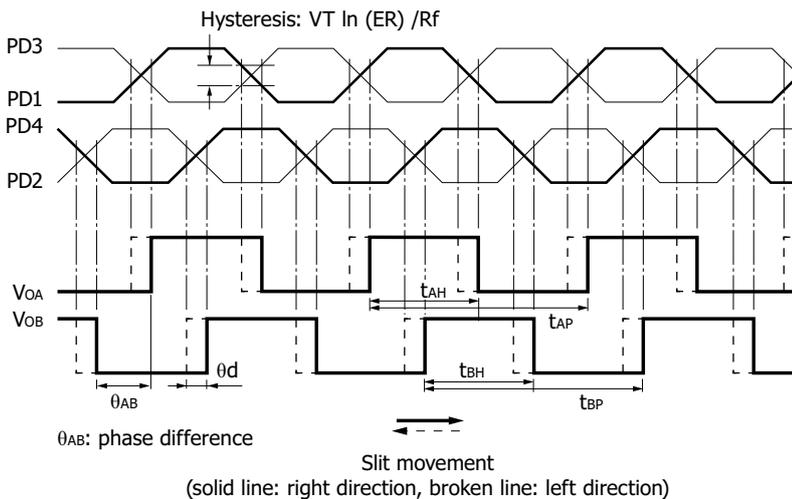
Recommended slit dimension (unit: mm, $t=0.1$)

(For center of slit plate position, see "Dimensional outline.")



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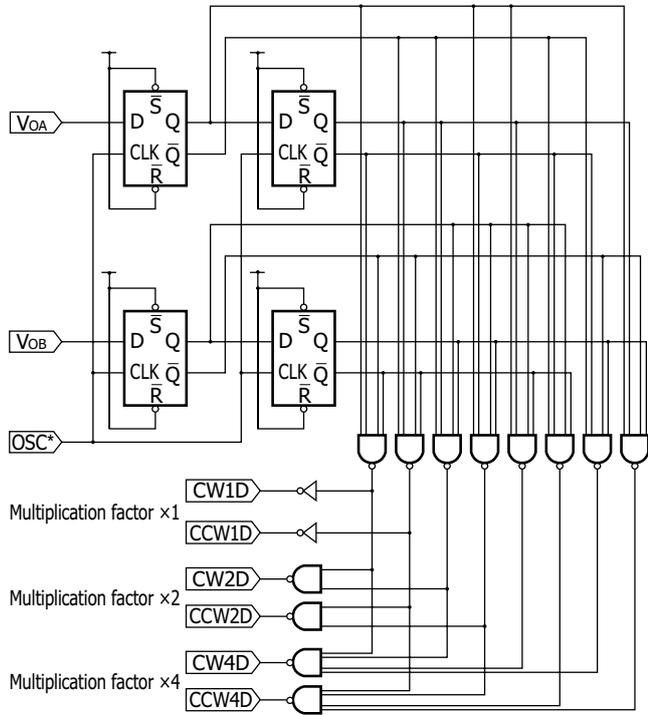
Timing chart



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Application circuit example (CW/CCW pulse signal generator circuit)

When the following application circuit is configured using the output (VOA, VOB) of the encoder module, the order of state transitions in VOA and VOB is detected at the OSC timing, and pulse signals are generated to the CWnD terminal in response to state transitions in the positive direction and to the CCWnD terminal in response to state transitions in the reverse direction (CWnD/CCWnD are output terminals for the multiplication factor $\times n$).

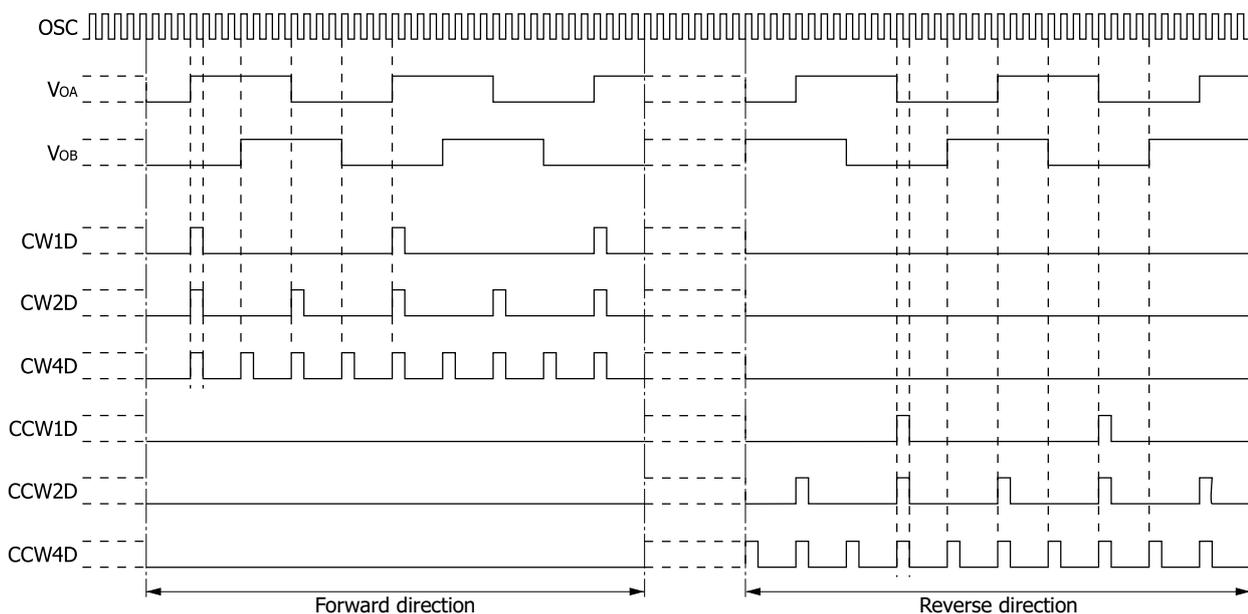


* External sampling signal

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Decoder output timing chart (when used with application circuit shown above)

A suitable sampling signal frequency is 40 or more times larger than the maximum frequency of one period of the VOA and VOB state transitions (in the following figure, 16 times for purposes of simplicity). Pulses appearing at each terminal are generated with a slight delay from the instant that the defined state transition occurs [maximum theoretical delay time = $1/\{2 \times \text{OSC frequency}\}$ (unit: cycles)]. Each of these signals is input to the up-count terminal and down-count terminal of the up/down counter. The amount of movement from the origin point can then be detected with a circuit that clears the up/down counter at origin position.



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Metal, ceramic, plastic products

Information described in this material is current as of October 2021.

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