Si8252x Data Sheet

4.0 A Symmetric Drive ISODrivers with 20 V VDDIH, Low Propagation Delay and High Transient Immunity.

The Si8252x combines two isolated drivers into a single package for high power applications. These drivers can operate with a 4.5 V – 20 V input VDD and a maximum drive supply voltage of 30 V.

The Si8252x is ideal for driving power MOSFETs and IGBTs used in a wide variety of switched power and motor control applications. These drivers utilize Silicon Labs' proprietary silicon isolation technology, supporting up to 5 kVRMS for 1 minute isolation voltage. This technology enables high CMTI (125 kV/µs), lower prop delays and skew, reduced variation with temperature and age and tighter part-to-part matching.

The unique architecture of the output stage features a booster device that provides a higher pull up capability at the Miller plateau region of the load power switch to support faster turn-on times. This driver family also offers some unique features such as over-temperature protection, output UVLO fault detection, dead time programmability and fail-safe drivers with default low in case of loss of input side power. The Si8252x family offers longer service life and dramatically higher reliability compared to opto-coupled gate drivers.

Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Solar and industrial inverters

Safety Approval (Pending)

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA certification conformity
  - IEC 60950-1, 62368-1 (reinforced insulation)
- VDE certification conformity
  - VDE 0884-10 (reinforced)
  - EN 60950-1, 62368-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- Two isolated drivers in one package
  - Up to 5 kV_{RMS} isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- EN pin for enhanced safety or DIS pin option
- Extended VDDIH
  - 4.5 V – 20V
- 4.0 A sink/source peak output
- High electromagnetic immunity
- 30 ns max propagation delay
- Transient immunity: >125 kV/µs
- Programmable dead time
  - 40–600 ns
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-14 WB
- AEC-Q100 qualified

1. Ordering Guide

Table 1.1. Si8252x Ordering Guide

Ordering Part Number	Configuration	Output UVLO (V)	Enable / Disable	Package Type	Isolation Rating (kVrms)
Si82520AD-IS3	HS/LS, VIA/VIB	5	DIS	SOIC-14 WB	5
Si82520BD-IS3	HS/LS, VIA/VIB	8	DIS	SOIC-14 WB	5
Si82520CD-IS3	HS/LS, VIA/VIB	12	DIS	SOIC-14 WB	5
Si82521AD-IS3	HS/LS, VIA/VIB	5	EN	SOIC-14 WB	5
Si82521BD-IS3	HS/LS, VIA/VIB	8	EN	SOIC-14 WB	5
Si82521CD-IS3	HS/LS, VIA/VIB	12	EN	SOIC-14 WB	5

1. All products are rated at 4 A sink and source output drive current max.
2. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
3. “Si” and “SI” are used interchangeably.
4. All HS/LS drivers have built-in overlap protection while the single and dual drivers do not.

Table of Contents

2. System Overview

2.1 Functional Description

The operation of an Si8252x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si8252x channel is shown in the figure below.

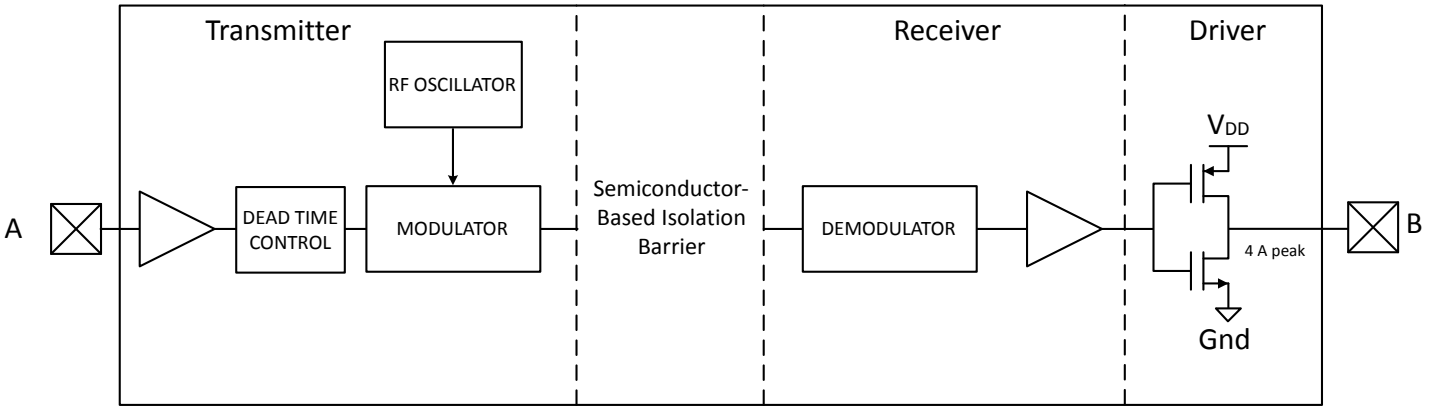


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

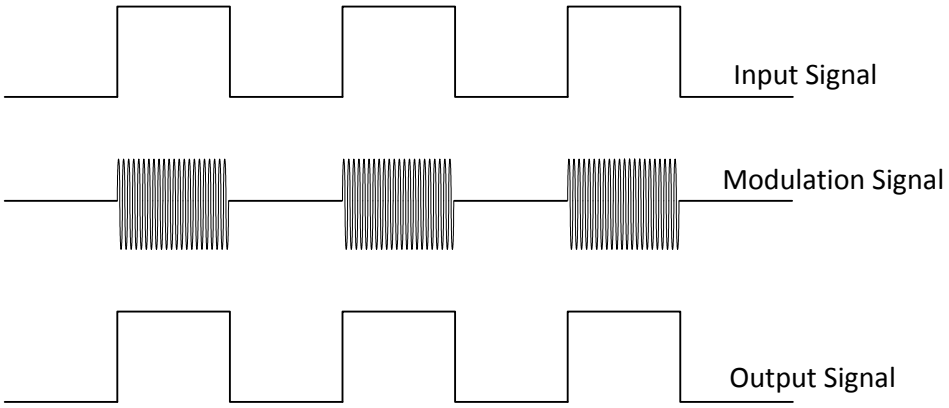


Figure 2.2. Modulation Scheme

2.2 Family Overview and Logic Operation During Startup

The Si8252x family of isolated drivers are high-side/low-side drivers.

2.2.1 Device Behavior

The following are truth tables for the Si8252x families.

Table 2.1. Si8252x Truth Table

VIA	VIB	DIS / EN[1]	VDDIH	VDDA	VDDB	VOA	VOB	Notes
H	L	L / H	P	P	P	H	L	
L	H	L / H	P	P	P	L	H	
H	H	L / H	P	P	P	L	L	
L	L	L / H	P	P	P	L	L	
X	X	H / L or NC	P	P	P	L	L	Device disabled
X	X	X	UP[2]	P	P	L	L	Fail-safe output when VDDIH un-powered
H	X	L / H	P	P	UP	H	UD[3]	VOB depends on VDDB state
L	X	L / H	P	P	UP	L	UD[3]	
X	H	L / H	P	UP	P	UD[3]	H	VOA depends on VDDA state
X	L	L / H	P	UP	P	UD[3]	L	

P = Powered, UP = Unpowered

Notes:

1. There are different product options available. For any one product, either EN or DIS is present.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDIH is unpowered. It is recommended that inputs be left unpowered when VDDIH is unpowered.
3. UD = undetermined if same side power is UP.

2.3 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si8252x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si8252x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance. For placement of the decoupling capacitors, it is recommended that the 0.1 µf capacitor should be placed as close as possible to the VDDA/B supply pins. The 10 µf capacitor can be a little farther away.

2.4 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in 2.4.2 Undervoltage Lockout, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDIH) is not present.

2.4.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

2.4.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si8252x input side enters UVLO when VDDIH ≤ $VDDIH_{UV-}$, and exits UVLO when VDDIH > $VDDIH_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si8252x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

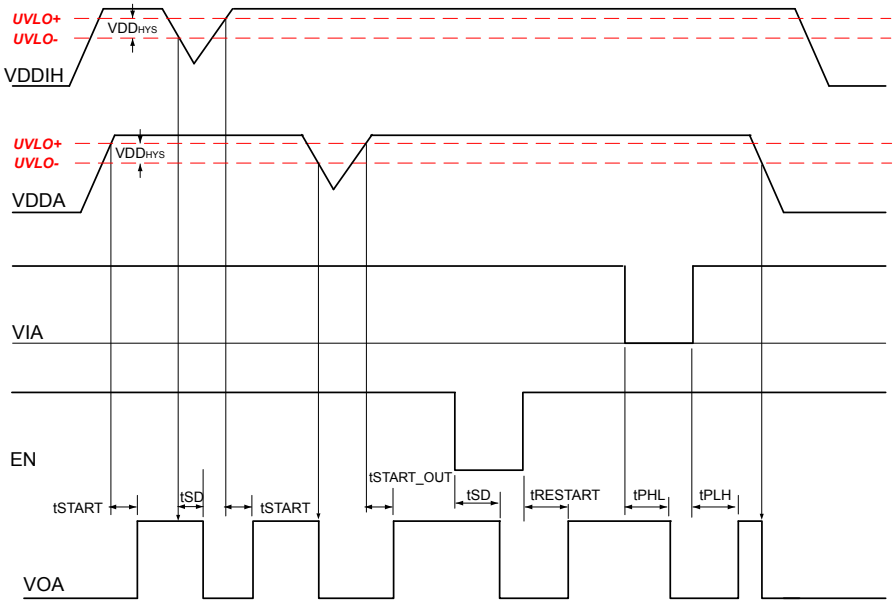


Figure 2.3. Si82521 Device Behavior During Normal Operation and Shutdown

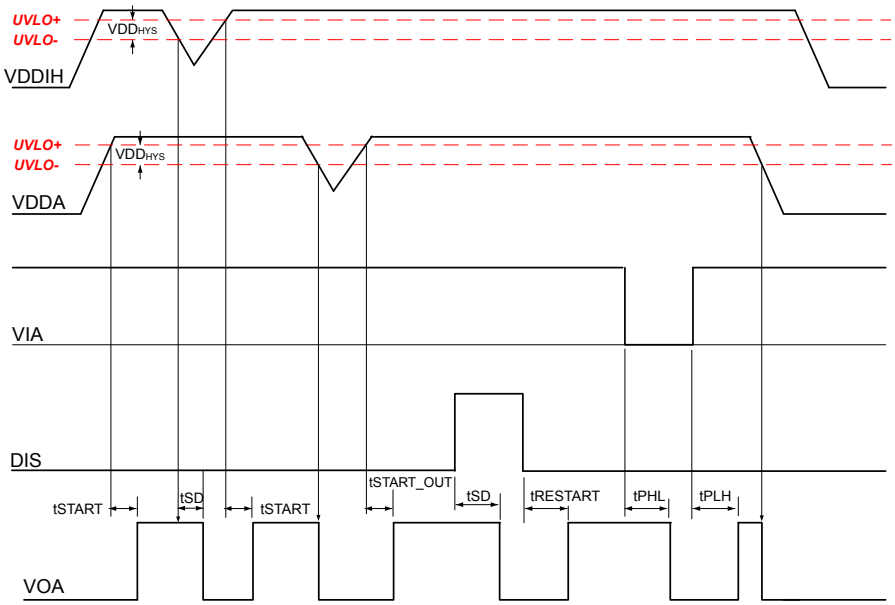


Figure 2.4. Si82520 Device Behavior During Normal Operation and Shutdown

2.5 Control Inputs

VIA and VIB inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high.

2.6 Enable Input

When brought low, the EN input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after EN = VIL and resumes within tRESTART after EN = VIH. The EN input has no effect if VDDIH is below its UVLO level (i.e., VOA, VOB remain low). There is an internal pull-down resistor of 100 kOhm on the EN pin.

2.7 Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after DISABLE =VIH and resumes within tRESTART after DISABLE = VIL or open. The DISABLE input has no effect if VDDIH is below its UVLO level (i.e., VOA, VOB remain low). There is an internal pull-down resistor of 100 kOhm on the DIS pin.

2.8 Programmable Dead Time and Overlap Protection

These high-side/low-side drivers include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When asserted, dead time is present only on output rising edges, when the other input is also high. If only one input is high, there is no dead time added to the output transition. Please see figure below for a graphical representation of dead time implementation. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per the equation below. The DT is measured as the time elapsed between VOA low to VOB high and vice versa.

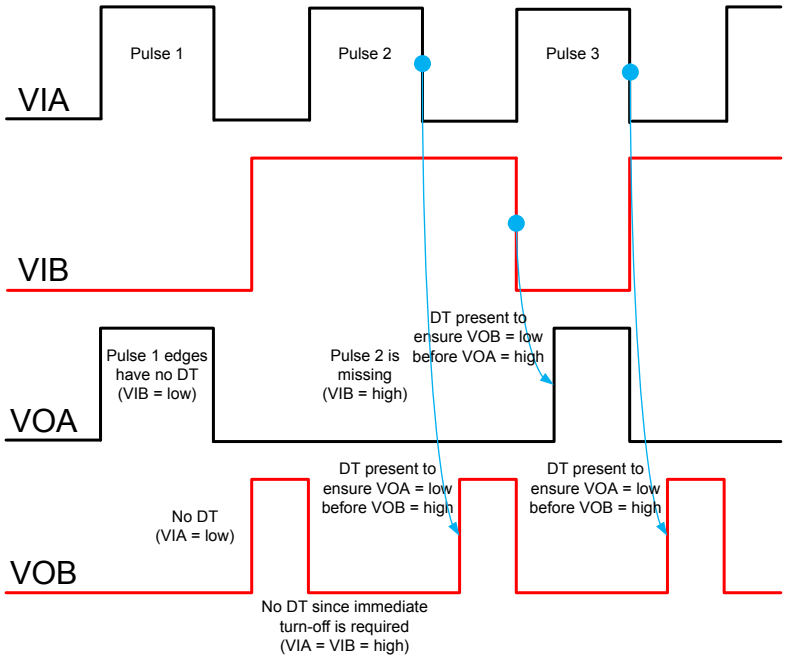


Figure 2.5. Dead Time Implementation & Behavior

DT ~ 5.4 x (RDT) + 14, where DT = Typical Dead Time in ns, RDT = Dead Time Resistor in kΩ

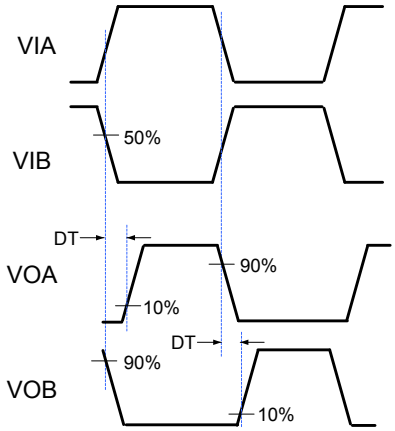


Figure 2.6. Dead Time Waveforms for High-Side/Low-Side Drivers

2.9 Thermal Protection

Si8252x has built-in temperature sensors for protection against high temperature resulting from overloading the driver, too high of an ambient temperature, or external component failures. If high internal temperature (>150 °C) is detected, the output is forced to low state.

2.10 Driver Output Booster Function

The output driver pull-up capability is enabled by two parallel drivers: a standard PMOS device and an NMOS helper transistor. The PMOS device provides a standard 1 A pull-up and the the DC pull-up when VO is close to VDD. The NMOS helper provides higher pull-up currents around the miller plateau of the driven power transistor, supporting fast turn-on times. See Figure 2.7 on page 8 for the internal architecture scheme and Figure 2.8 on page 8 for the pull-up current characteristics.

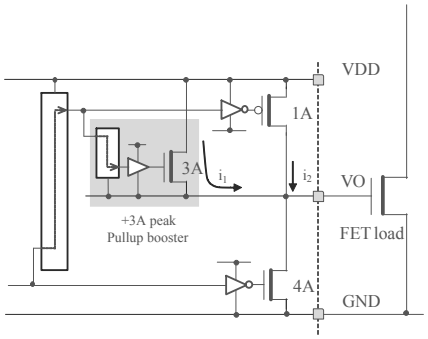


Figure 2.7. Pull-Up Booster Simplified Architecture

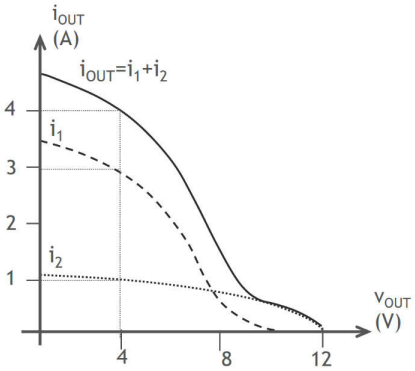


Figure 2.8. Pull-Up Current Characteristics, VDD = 12 V

3. Applications

The following examples illustrate typical circuit configurations using the Si8252x.

3.1 HS/LS Driver

The following figure shows the device configured as a HS/LS driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 Vdc between them.

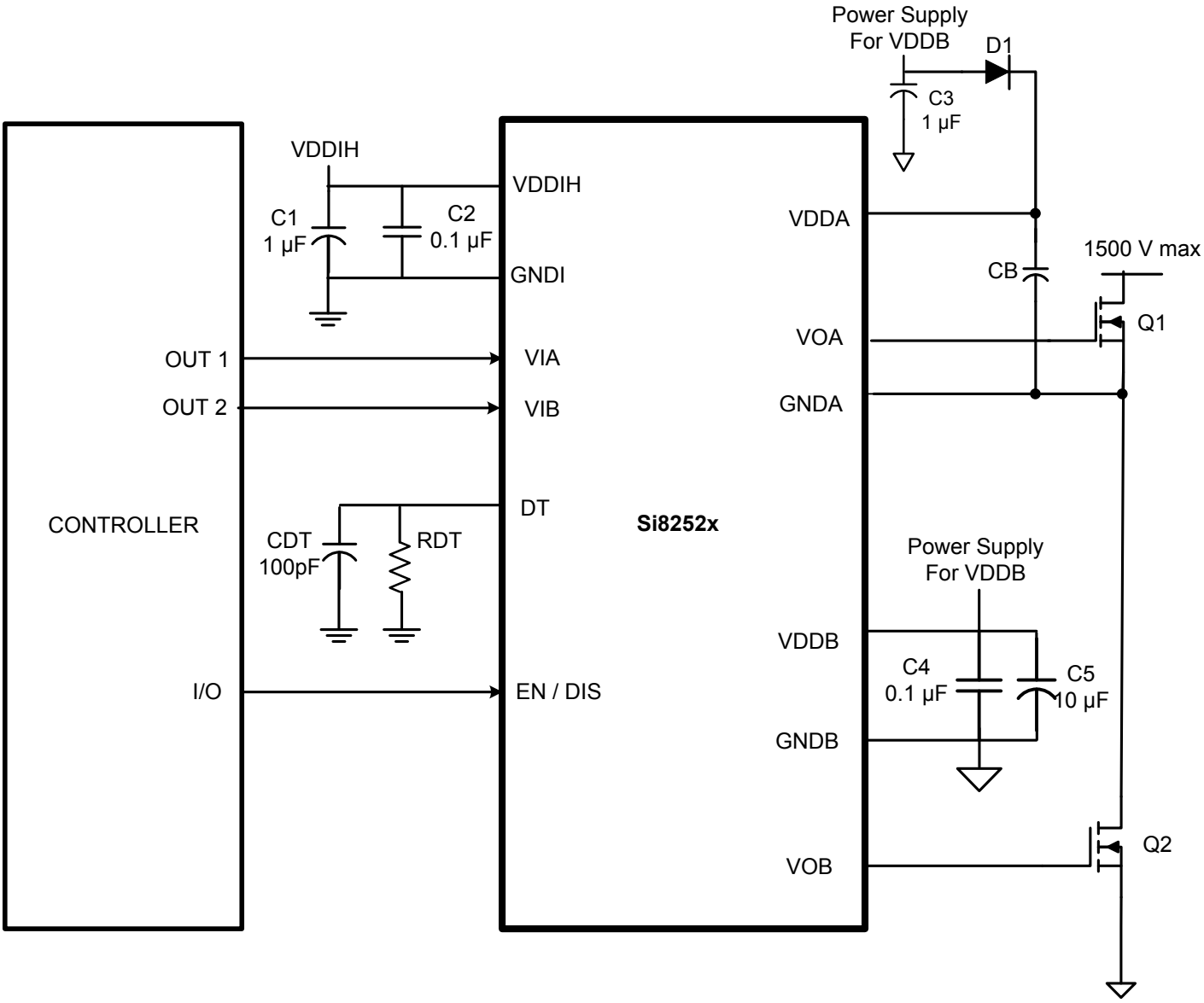


Figure 3.1. Si8252x with EN/DIS Pin Application Diagram

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver.

In the above figure, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si8252x requires VDDIH in the range of 4.5 to 20.0 V, while the VDDA and VDDB output side supplies must be between 5.5 and 30 V referred to their respective grounds. The boot-strap start up time will depend on the CB cap chosen. Also note that the bypass capacitors on the Si8252x should be located as close to the chip as possible.

4. Electrical Characteristics

Table 4.1. Electrical Characteristics[1, 2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDIH		4.5		20	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA andGNDA, and VDDB and GNDB	5.5	—	30	V
Input Supply Quiescent Current EN = 0	IDDI(Q)		—	1.3	2.0	mA
Input Supply Active Current (with one channel active)	IDDI	freq = 1 MHz	—	2.2	3.3	mA
Input Supply Active Current (with both channels active)	IDDI	freq = 1 MHz	—	3.6	4.75	mA
Output Supply Quiescent Current, per channel EN = 0	IDDA(Q), IDDB(Q)		—	2.3	2.8	mA
Output Supply Active Current, per channel	IDDA/B	Input freq = 1 MHz, no load	—	5.6	9.0	mA
Input Pin Leakage Current, VIA, VIB	IVIA, IVIB		–10	—	+10	µA
Input Pin Leakage Current, EN, DIS	IENABLE, IDISABLE		–40	—	+40	µA
Logic High Input Threshold	VIH	TTL Levels	1.6	1.8	2.0	V
Logic Low Input Threshold	VIL	TTL Levels	0.8	1	1.2	V
Input Hysteresis	VIHYST			800	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	VDDA, VDDB – 0.064	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Source Current	IOA(SCL), IOB(SCL)	CL = 220 nF	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	CL = 220 nF	—	4.0	—	A
Output Sink Resistance	RON(SINK)		—	1.0	—	Ω
Output Source Resistance	RON(SOURCE)		—	4.2	—	Ω
VDDIH Undervoltage Threshold	VDDIHUV+	VDDIH rising	3.2	3.7	4.4	V
VDDIH Undervoltage Threshold	VDDIHUV–	VDDIH falling	2.7	3.55	4.0	V
VDDIH Lockout Hysteresis	VDDIHHYS		70	500	—	mV
VDDA, VDDB Undervoltage Threshold	VDDAUV+, VDDBUV+	VDDA, VDDB rising				V
5 V Threshold			4.5	4.9	5.3	
8 V Threshold			7.5	8.1	8.8	
12 V Threshold			11.3	12.2	13.4	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDDA, VDDB Undervoltage Threshold	VDDAUV–, VDDBUV–	VDDA, VDDB falling				V
5 V Threshold			4.3	4.7	5.0	
8 V Threshold			7.0	7.6	8.2	
12 V Threshold			10.3	11.1	12.0	
VDDA, VDDB Lockout Hysteresis	VDDAHYS, VDDBHYS	UVLO = 5 V	150	220	—	mV
		UVLO = 8 V	450	550	—	
		UVLO = 12 V	950	1200	—	
AC Specifications						
UVLO Fault Shutdown Time		VDDAUV– to VOA low VDDBUV– to VOB low	—	10	—	ns
Minimum Pulse Width	PW_{min}		—	30	—	ns
Propagation Delay VDDA/B = 12 V CL = 0 pF	t_{pHL}, t_{pLH}		10	19	30	ns
Output Channel to Channel Skew	t_{PSK}			3	5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	10	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	VDDA/B = 12 V CL = 0 pF	—	2.7	5.60	ns
Programmed Dead Time	DT	RDT = 6 kΩ	39	48	57	ns
		RDT = 10 kΩ	58	72	86	
		RDT = 100 kΩ	502	557	615	
Output Rise and Fall Time	tR,tF	CL = 200 pF	—	—	12	ns
Shutdown Time from ENable False (or DISable true)	tSD		—	—	30	ns
Restart Time from ENable True (or DISable false)	tRESTART		—	—	30	ns
Device Start-up Time Input	tSTART	Time from VDDIH_ = VDDIH_UV+ to VOA, VOB = VIA, VIB	—	40	—	µs
Device Start-up Time Output	tSTART_OUT	Time from VDDA/B = VDDA/ B_UV+ to VOA, VOB = VIA, VIB	—	60	—	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDIH or 0 V VCM = 1500 V	125	150	—	kV/µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 4.5 V < VDDIH < 20 V; 5.5 V < VDDA, VDDB < 30 V; TA = –40 to +125 °C.
2. Typical specs at 25 °C, VDDA = VDDB = 12 V for 5 V and 8 V UVLO devices, otherwise 15 V.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Test Circuits

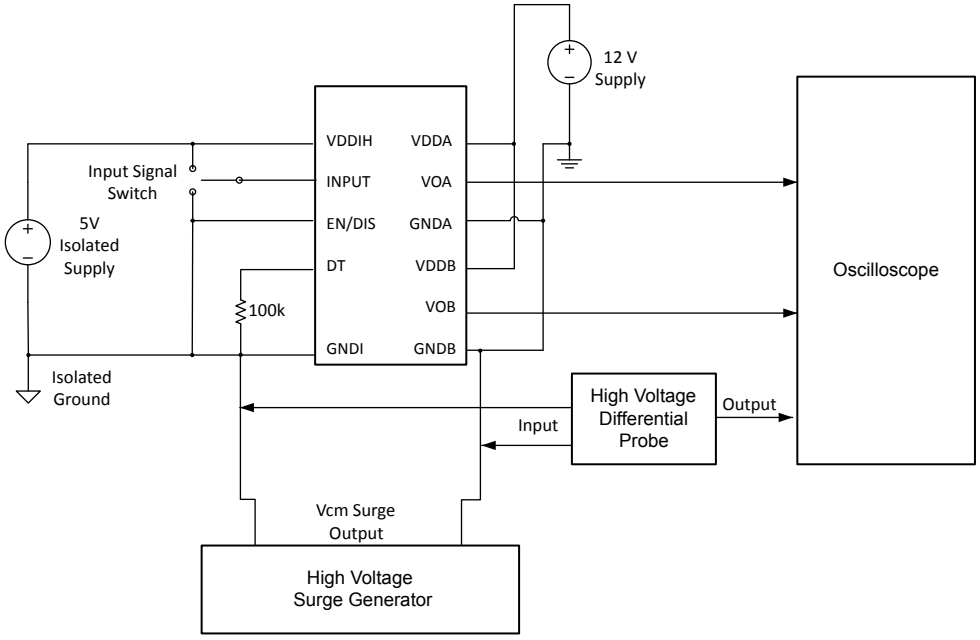


Figure 4.1. Common Mode Transient Immunity (CMTI) Test Circuit

Table 4.2. Regulatory Information (Pending)[1, 3, 4]

CSA
The Si8252x is certified under CSA, see Master Contract Number 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8252x is certified according to VDE 0884-10. For more details, see Certificate 40037519.
VDE 0884-10: Up to 891 V_{peak} for reinforced insulation working voltage.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si8252x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si8252x is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1sec. 2. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1sec. 3. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1sec. 4. For more information, see Chapter 1. Ordering Guide.

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			SOIC-14 WB 5 kVrms	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	mm
Nominal External Tracking (Creepage)[1]	CPG		8.0	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.016	mm
Tracking Resistance	CTI or PTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.7	pF
Input Capacitance[3]	C_I		3.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values.
2. To determine resistance and capacitance, the device is converted into a 2-terminal device. All pins on side 1 and all pins on side 2 are shorted.
3. Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification
		SOIC-14 WB
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV
	Rated Mains Voltages < 400 V_{RMS}	I-IV
	Rated Mains Voltages < 600 V_{RMS}	I-IV

Table 4.5. VDE0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
			SOIC-14 WB	
Maximum Working Insulation Voltage	V_{IORM}		891	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	V peak
Transient Overvoltage	V_{IOTM}	t = 60 s	8000	V peak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage with rise/decay time of 1.2 µs/50 µs	6250 Tested with 10,000 V	V peak
Pollution Degree (DIN VDE 0110, Table 4.1 Electrical Characteristics[1, 2] on page 10)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:**
1. Maintenance of the safety data is ensured by protective circuits. The Si8252x provides a climate classification of 40/125/21.

Table 4.6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	SOIC-14 WB	Unit
Safety Temperature	T_S		150	°C
Safety Current	I_S	θ_{JA} Refer to package specific values for junction to air thermal resistance in Table 4.7 below V_{DDIH} = 5.5 V, V_{DDA} = V_{DDB} = 30 V, T_J = 150 °C, T_A = 25 °C	70	mA
Device Power Dissipation[2]	P_D		1.84	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 4.2 SOIC-14 WB Thermal Derating Curve, Dependence of Safety Limiting Values on page 16.
2. Si8252x is tested with CL = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 4.7. Thermal Characteristics

Parameter	Symbol	SOIC-14 WB	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	59	°C/W

Table 4.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Ambient Temperature under Bias	TA	–40	+125	°C
Storage Temperature	TSTG	–65	+150	°C
Junction Temperature	TJ	—	+150	°C
Input-side Supply Voltage	VVDIH	–0.6	24	V
Driver-side Supply Voltage	VDDA, VDDB	–0.6	36	V
Voltage on any Pin with respect to Ground	VIA, VIB Transient for 50 ns	–5.0	VDD + 0.5	V
	VIA, VIB, EN, DIS,DT	-0.6	VDD + 0.5	
Peak Output Current (tPW = 10 µs, duty cycle = 0.2%)	IOPK	—	6.0	A
Lead Solder Temperature (10 s)		—	260	°C
ESD per AEC-Q100	HBM	—	4	kV
	CDM	—	0.5	kV
Maximum Isolation (Input to Output) (1 s) SOIC-14 WB		—	6500	VRMS
Maximum Isolation (Output to Output) (1 s) SOIC-14 WB		—	1500	VRMS

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

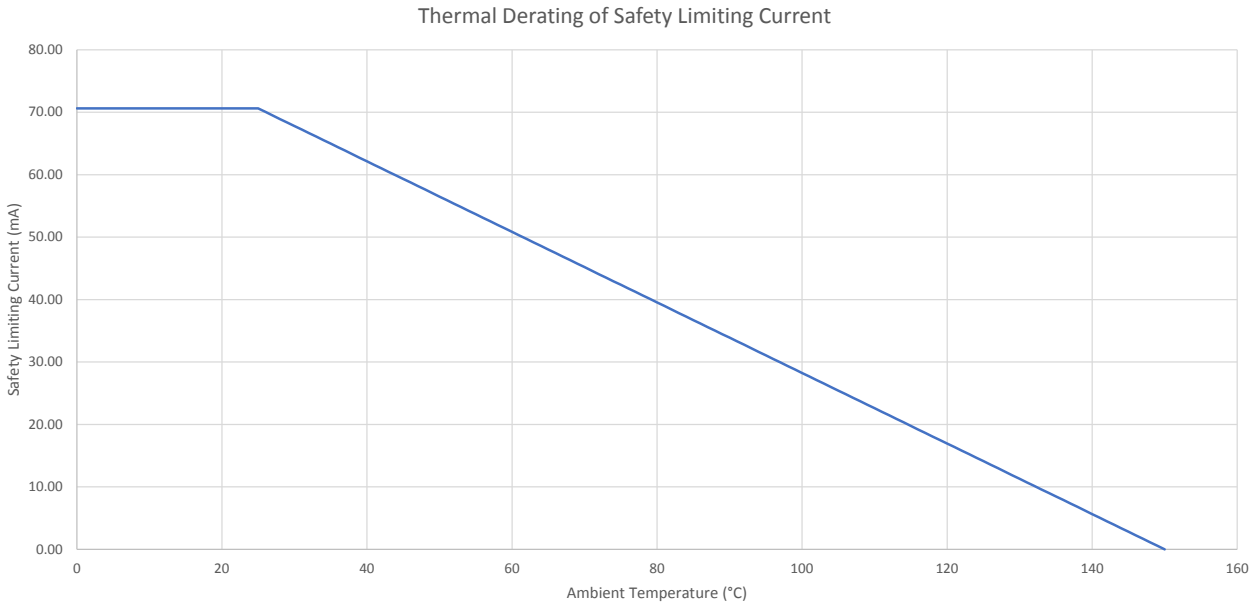


Figure 4.2. SOIC-14 WB Thermal Derating Curve, Dependence of Safety Limiting Values

4.1 Typical Operating Characteristics

The typical performance characteristics depicted in this subsection are for information purposes only. Refer to Chapter 4. Electrical Characteristics for actual specification limits.

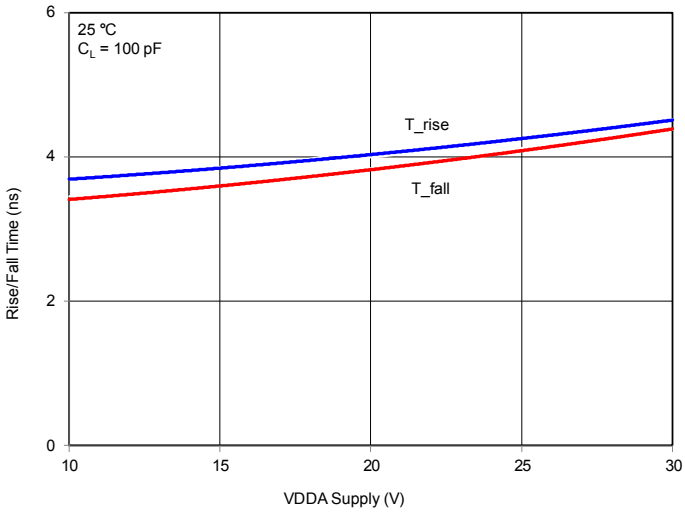


Figure 4.3. Rise/Fall Time vs. Supply Voltage

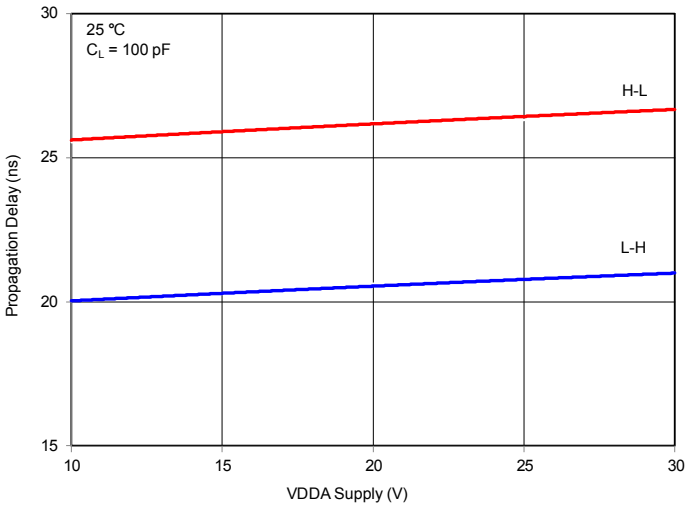


Figure 4.4. Propagation Delay vs. Supply Voltage

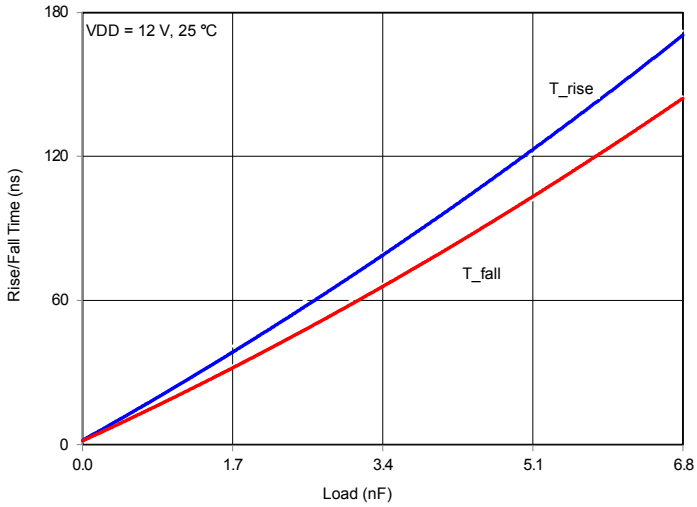


Figure 4.5. Rise/Fall Time vs. Load

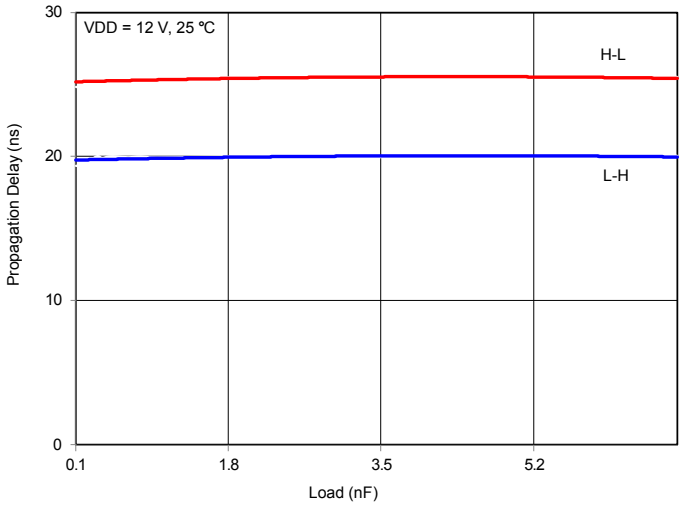


Figure 4.6. Propagation Delay vs. Load

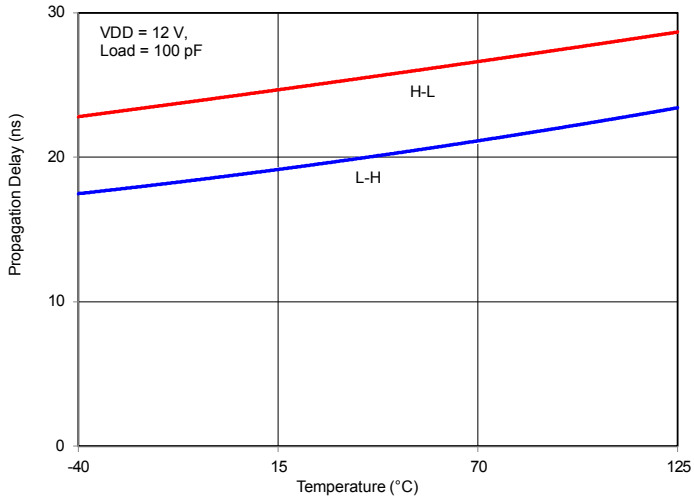


Figure 4.7. Propagation Delay vs. Temperature

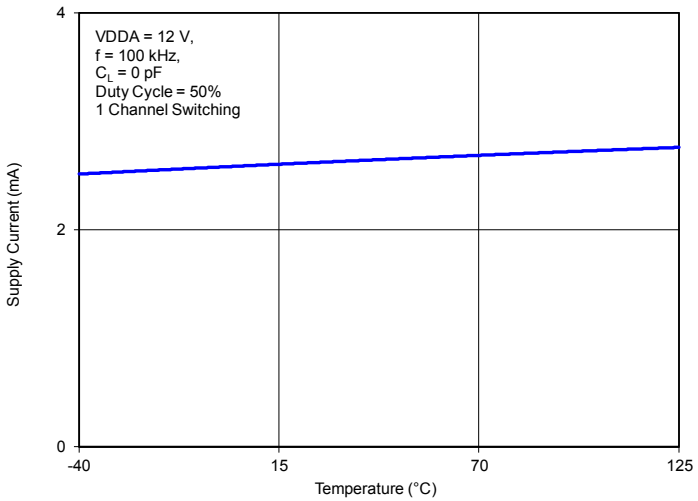


Figure 4.8. Supply Current vs. Temperature

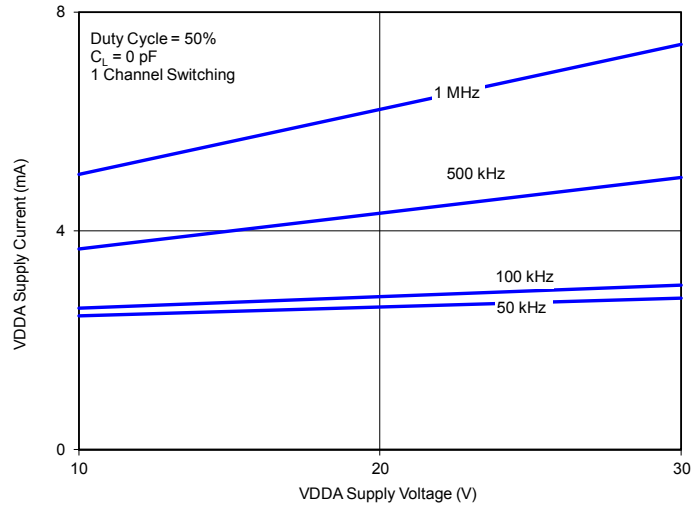


Figure 4.9. Supply Current vs. Supply Voltage (C_L = 0 pF)

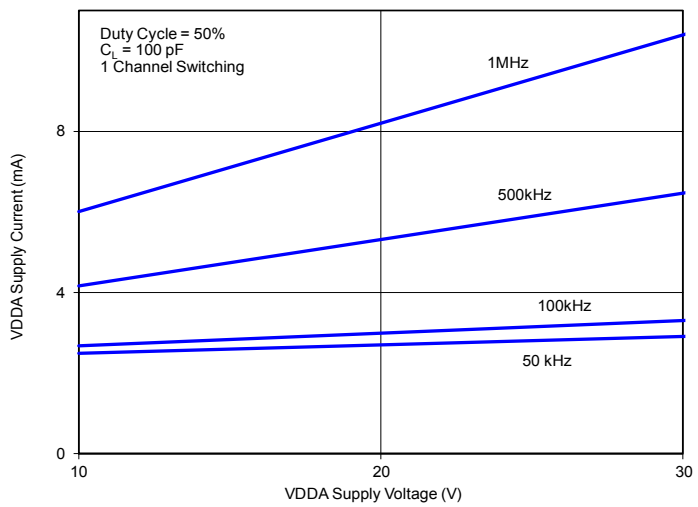


Figure 4.10. Supply Current vs. Supply Voltage (C_L = 100 pF)

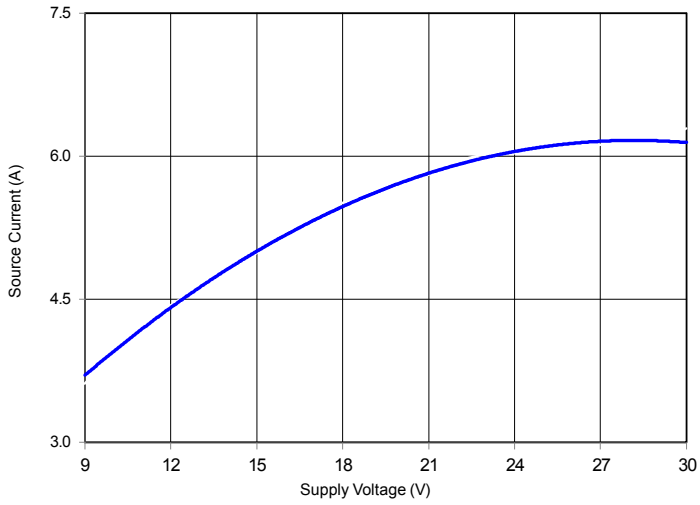


Figure 4.11. Output Source Current vs. Supply Voltage

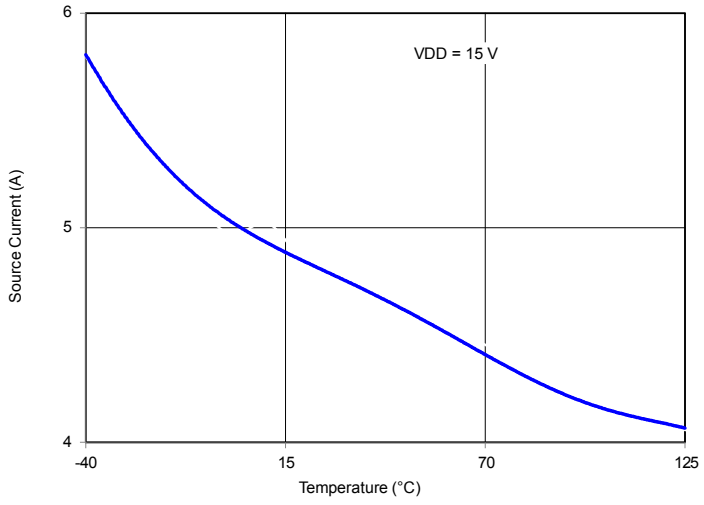


Figure 4.12. Output Source Current vs. Temperature

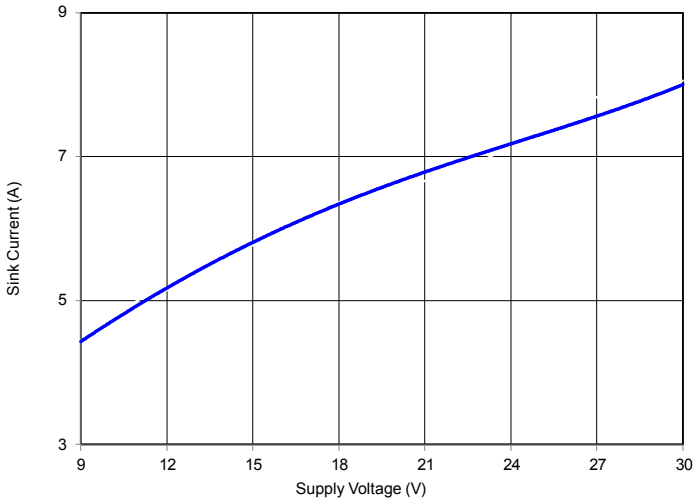


Figure 4.13. Output Sink Current vs. Supply Voltage

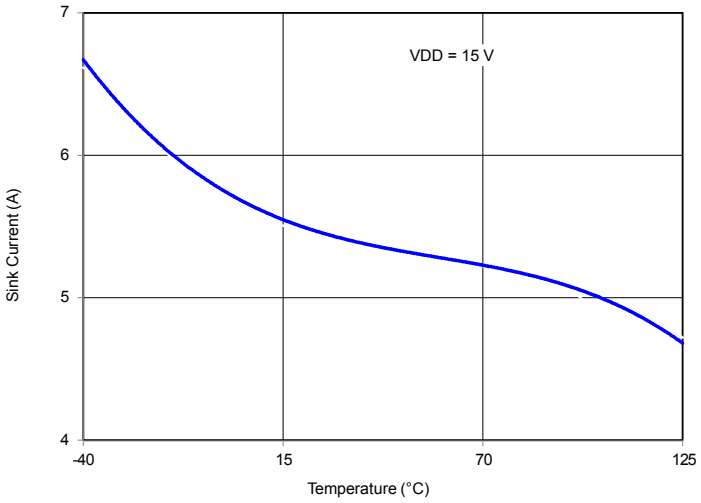


Figure 4.14. Output Sink Current vs. Temperature

5. Top-Level Block Diagrams

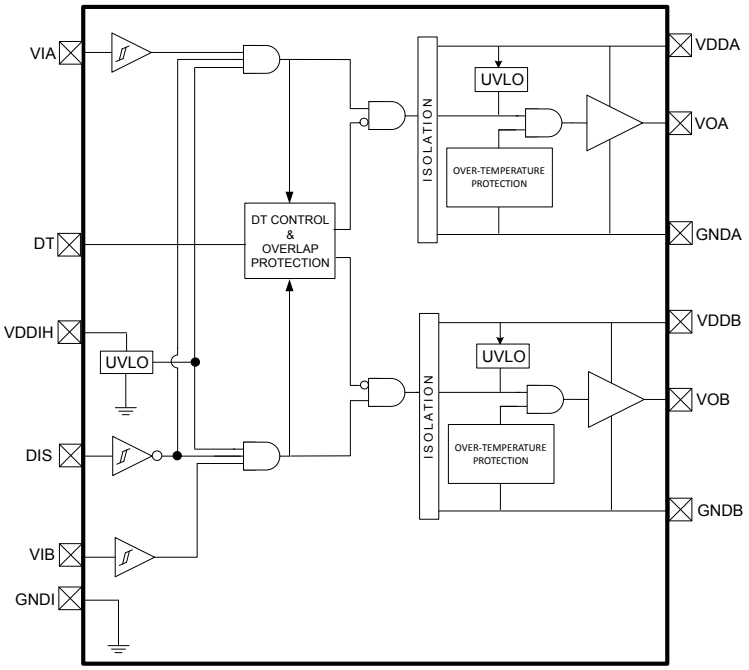


Figure 5.1. Si82520 HS/LS Isolated Drivers with DIS

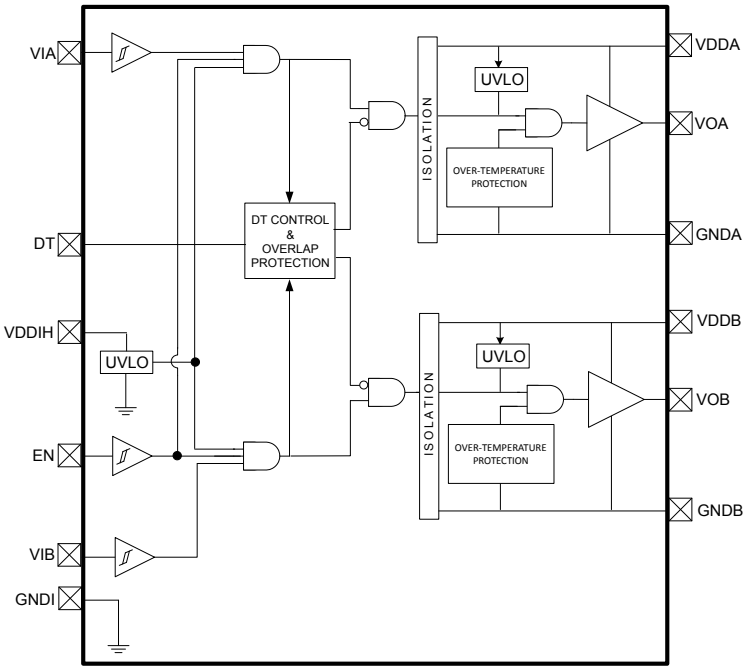


Figure 5.2. Si82521 HS/LS Isolated Drivers with EN

6. Pin Descriptions

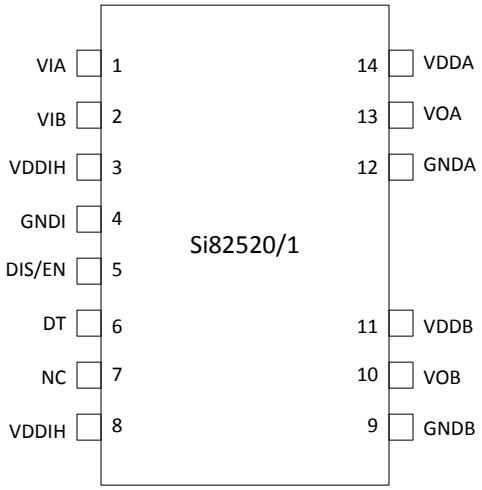


Figure 6.1. Si82520/1 SOIC-14 WB

Table 6.1. Pin Descriptions

Pin Name	Description
VIA	Non-inverting logic input terminal for Driver A.
VIB	Non-inverting logic input terminal for Driver B.
VDDIH	High Voltage Input-side power supply terminal.
GNDI	Input-side ground terminal.
EN	Device ENABLE. When asserted, this input enables normal operation of the device. When low or NC, this input unconditionally drives outputs VOA, VOB LOW. When high, device is enabled to perform in normal operating mode. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DIS	Device DISABLE. When asserted, this input unconditionally drives outputs VOA, VOB LOW. When low or open, device is enabled to perform in normal operating mode. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB.
NC	No connection.
GNDB	Ground terminal for Driver B.
VOB	Driver B output (low-side driver).
VDDB	Driver B power supply voltage terminal; connect to a source.
GNDA	Ground terminal for Driver A.
VOA	Driver A output (high-side driver)
VDDA	Driver A power supply voltage terminal; connect to a source.

7. Package Outlines

7.1 14-Pin Wide Body SOIC (SOIC-14 WB)

The figure below illustrates the package details for the Si8252x in a 14-pin wide-body SOIC. The table below lists the values for the dimensions shown in the illustration.

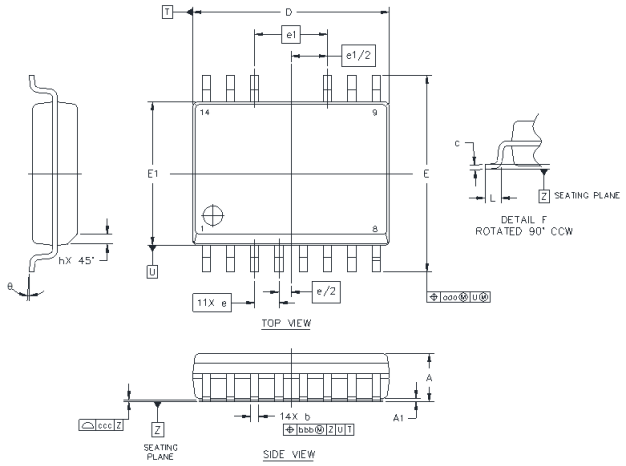


Figure 7.1. 14-pin Small Outline Integrated Circuit (SOIC) Package

Table 7.1. Package Diagram Dimensions

Dimension	MIN	MAX
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.35	0.49
c	0.23	0.32
D	10.15	10.45
E	10.05	10.55
E1	7.40	7.60
e	1.27 BSC	
e1	3.81 BSC	
L	0.40	1.27
h	0.25	0.75
Θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8. Land Patterns

8.1 14-Pin Wide Body SOIC

The figure below illustrates the recommended land pattern details for the Si8252x in a 14-pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

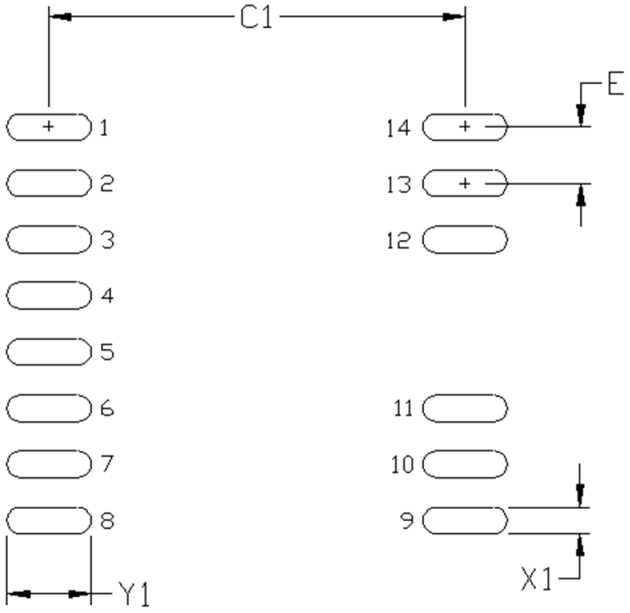


Figure 8.1. 14-Pin WB SOIC Land Pattern

Table 8.1. 14-Pin WB SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.70
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1 14-Pin Wide Body SOIC

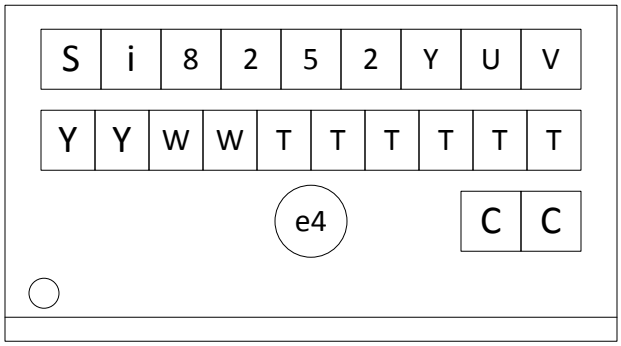


Table 9.1. Top Marking Explanation (14-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si82520/1 = ISODriver product series (HS/LS drivers) with high voltage VDDIH Y = Enable scheme • 0 = Disable pin option • 1 = Enable pin option U = UVLO level: A, B, C (applies to both product series) • A = 5 V • B = 8 V • C = 12 V V = Isolation rating: • D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.7 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

10. Revision History

Revision 0.6

September 2020

- Updated θ_{JA} for WB.

Revision 0.5

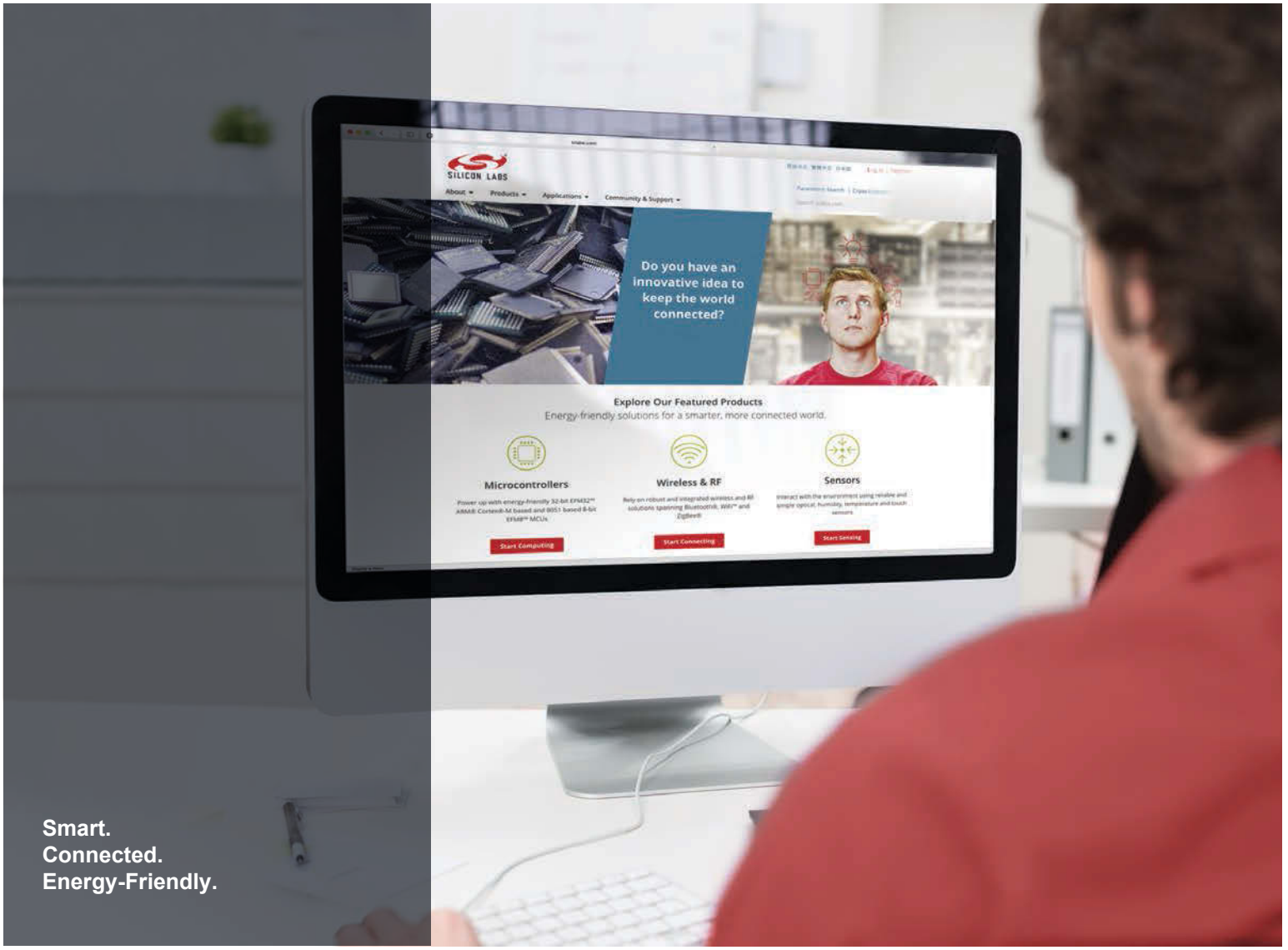
September 2019

- Formatting and typo corrections.

Revision 0.2

January 2019

- Separated datasheet from Si8252x prodcuts from Si823Hx products



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